15 DEVICES COVER MILITARY, INDUSTRIAL, AND COMMERCIAL TEMPERATURE RANGES

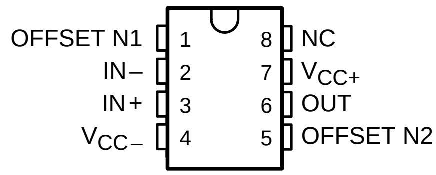
- **Very Low Power Consumption**
- **Typical Supply Current . . . 200 μA (per Amplifier)**
- **Wide Common-Mode and Differential Voltage Ranges**
- **Low Input Bias and Offset Currents**
- **Common-Mode Input Voltage Range Includes V_{CC+}**
- **Output Short-Circuit Protection**
- **High Input impedance . . . JFET-Input Stage**
- **Internal Frequency Compensation**
- **Latch-Up-Free Operation**
- **High Slew Rate . . . 3.5 V/μs Typ**

description

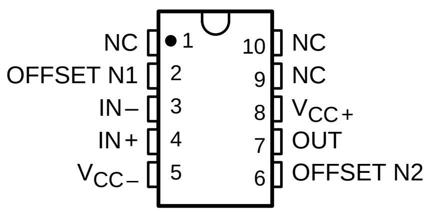
The JFET-input operational amplifiers of the TL06_ series are designed as low-power versions of the TL08_ series amplifiers. They feature high input impedance, wide bandwidth, high slew rate, and low input offset and bias currents. The TL06_ series feature the same terminal assignments as the TL07_ and TL08_ series. Each of these JFET-input operational amplifiers incorporates well-matched, high-voltage JFET and bipolar transistors in a monolithic integrated circuit.

The C-suffix devices are characterized for operation from 0°C to 70°C. The I-suffix devices are characterized for operation from –40°C to 85°C, and the M-suffix devices are characterized for operation over the full military temperature range of –55°C to 125°C.

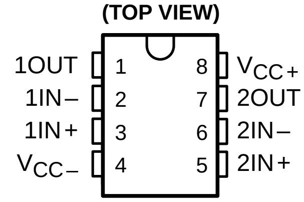
TL061, TL061A, TL061B
D, JG, P, OR PW PACKAGE
(TOP VIEW)



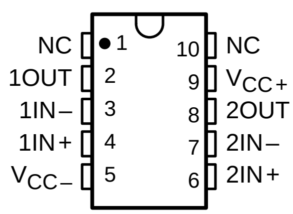
TL061 . . . U PACKAGE
(TOP VIEW)



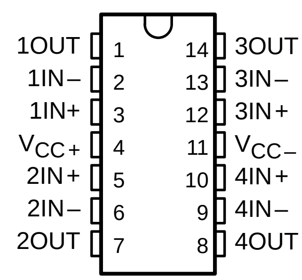
TL062, TL062A, TL062B
D, JG, P, OR PW PACKAGE
(TOP VIEW)



TL062 . . . U PACKAGE
(TOP VIEW)

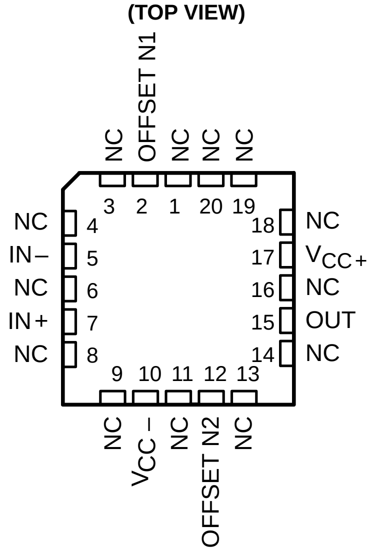


TL064 . . . D, J, N, PW, OR W PACKAGE
TL064A, TL064B . . . D OR N PACKAGE
(TOP VIEW)

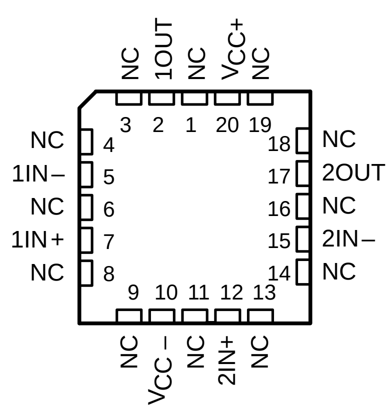


NC – No internal connection

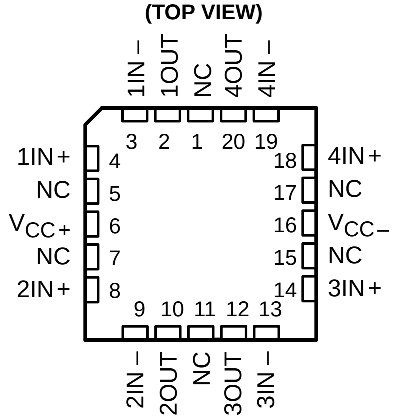
TL061 . . . FK PACKAGE
(TOP VIEW)



TL062 . . . FK PACKAGE
(TOP VIEW)



TL064 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

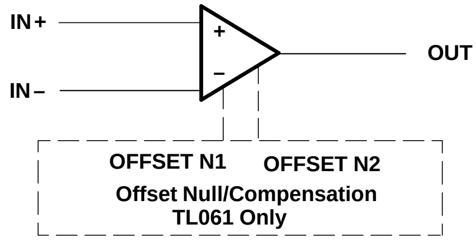
AVAILABLE OPTIONS

T_A	V_{IO}max AT 25°C	PACKAGED DEVICES					CHIP FORM (Y)
		SMALL OUTLINE (D008)†	SMALL OUTLINE (D014)†	PLASTIC DIP (N)	PLASTIC DIP (P)	TSSOP (PW)	
0°C to 70°C	15 mV 6 mV 3 mV	TL061CD TL061ACD TL061BCD			TL061CP TL061ACP TL061BCP	TL061CPW	TL061Y
	15 mV 6 mV 3 mV	TL062CD TL062ACD TL062BCD			TL062CP TL062ACP TL062BCP	TL062CPW	TL062Y
	15 mV 6 mV 3 mV		TL064CD TL064ACD TL064BCD	TL064CN TL064ACN TL064BCN		TL064CPW	TL064Y

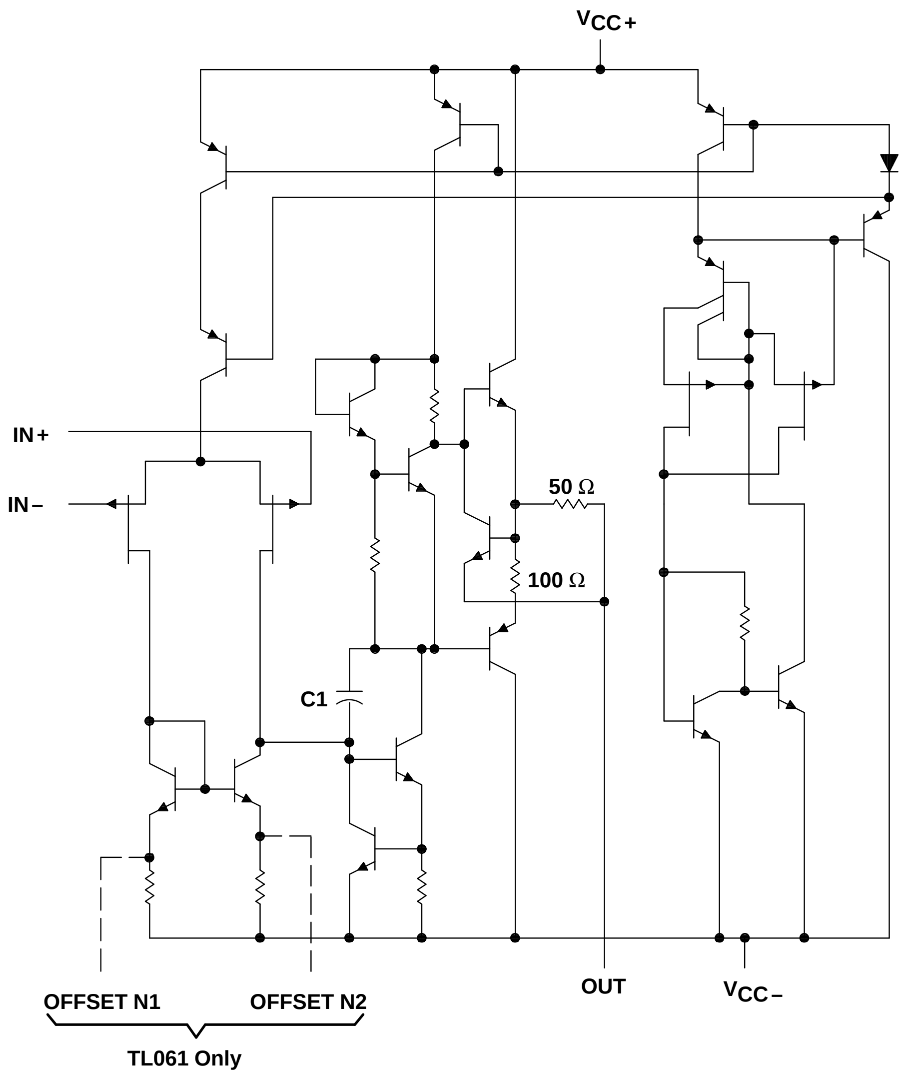
T_A	V_{IO}max AT 25°C	PACKAGE								
		SMALL OUTLINE (D008)†	SMALL OUTLINE (D014)†	CHIP CARRIER (FK)	CERAMIC DIP (J)	CERAMIC DIP (JG)	PLASTIC DIP (N)	PLASTIC DIP (P)	FLAT PACK (U)	FLAT PACK (W)
–40°C to 85°C	6 mV	TL061ID TL062ID	TL064ID				TL064IN	TL061IP TL062IP		
–55°C to 125°C	6 mV 6 mV 9 mV			TL061MFK TL062MFK TL064MFK	TL064MJ	TL061MJG TL062MJG			TL061MU TL062MU	TL064MW

† The D package is available taped and reeled. Add the suffix R to the device type (e.g., TL061CDR).

symbol (each amplifier)



schematic (each amplifier)

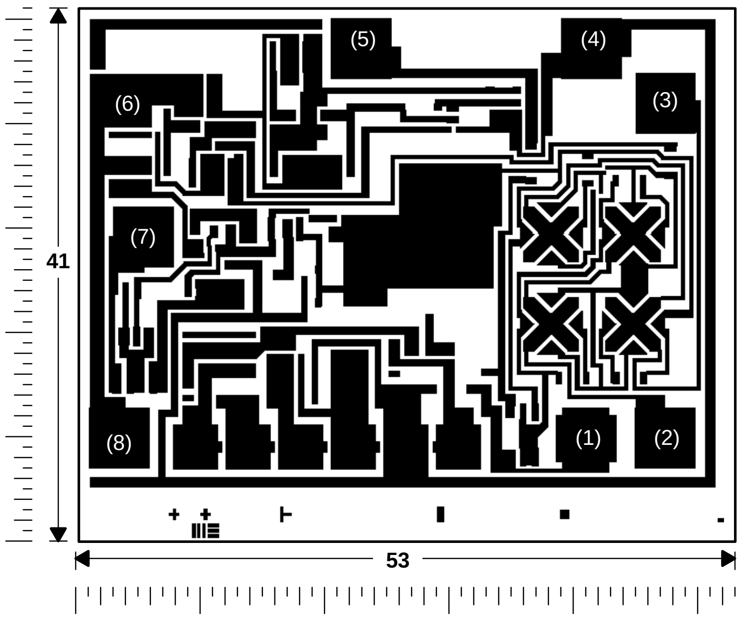


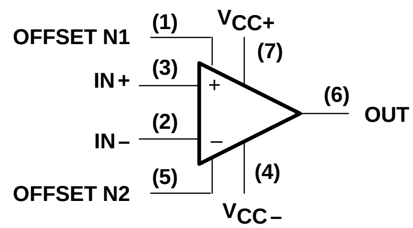
C1 = 10 pF on TL061, TL062, and TL064
Component values shown are nominal.

TL061Y chip information

This chip, when properly assembled, displays characteristics similar to the TL061. Thermal compression or ultrasonic bonding may be used on the doped-aluminum bonding pads. The chips may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





CHIP THICKNESS: 15 TYPICAL

BONDING PADS: 4 × 4 MINIMUM

$T_J$max = 150°C

TOLERANCES ARE ±10%.

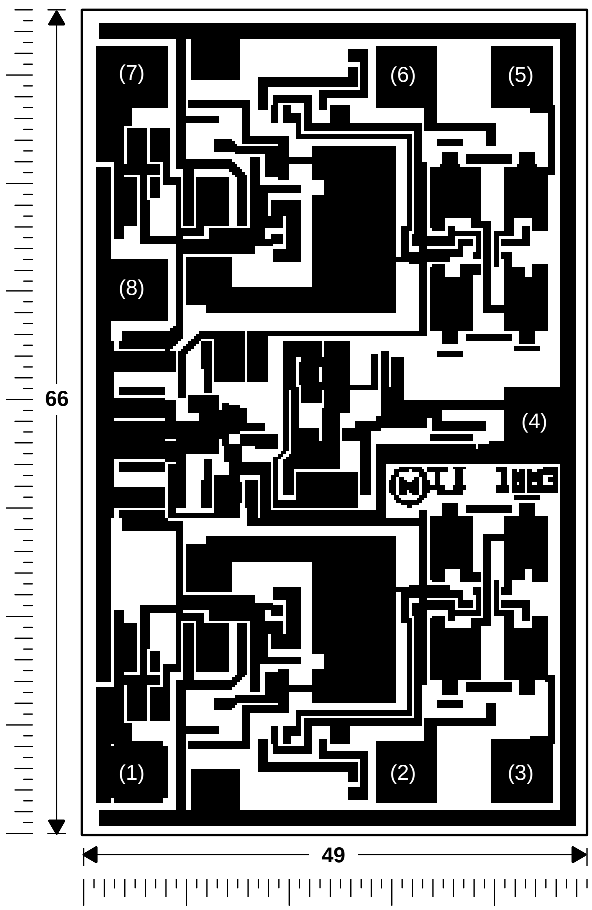
ALL DIMENSIONS ARE IN MILS.

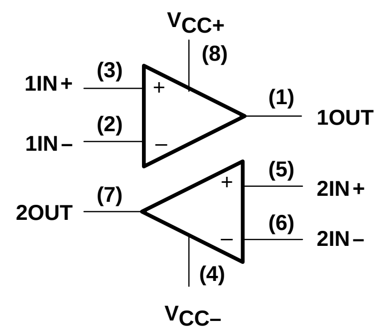
PIN (4) IS INTERNALLY CONNECTED TO BACKSIDE OF CHIP.

TL062Y chip information

This chip, when properly assembled, displays characteristics similar to the TL062. Thermal compression or ultrasonic bonding may be used on the doped-aluminum bonding pads. The chips may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





CHIP THICKNESS: 15 TYPICAL

BONDING PADS: 4 × 4 MINIMUM

$T_J$max = 150°C

TOLERANCES ARE ±10%.

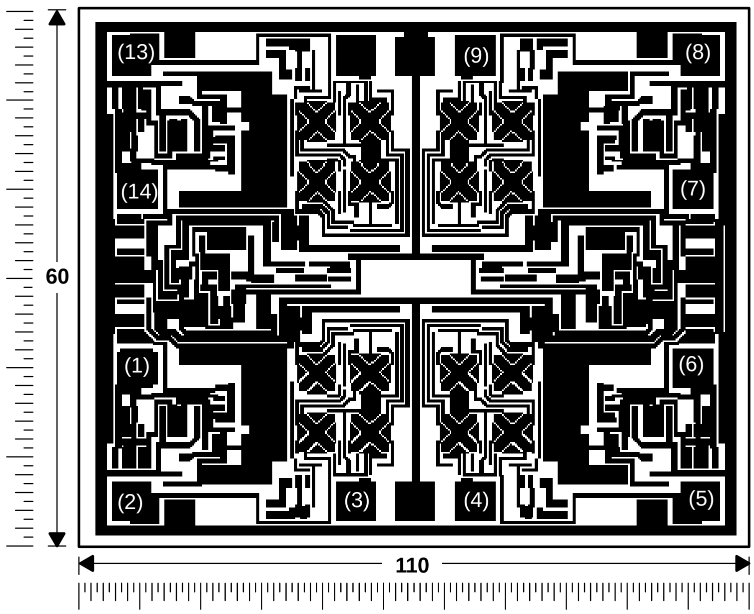
ALL DIMENSIONS ARE IN MILS.

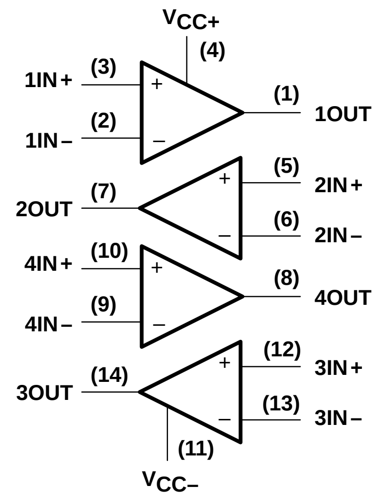
PIN (4) IS INTERNALLY CONNECTED TO BACKSIDE OF CHIP.

TL064Y chip information

This chip, when properly assembled, displays characteristics similar to the TL064. Thermal compression or ultrasonic bonding may be used on the doped-aluminum bonding pads. The chips may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





CHIP THICKNESS: 15 TYPICAL

BONDING PADS: 4 × 4 MINIMUM

$T_J$max = 150°C

TOLERANCES ARE ±10%.

ALL DIMENSIONS ARE IN MILS.

PIN (11) IS INTERNALLY CONNECTED TO BACKSIDE OF CHIP.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

		TL06_C TL06_AC TL06_BC	TL06_I	TL06_M	UNIT
Supply voltage, V_{CC+} (see Note 1)		18	18	18	V
Supply voltage, V_{CC-} (see Note 1)		–18	–18	–18	V
Differential input voltage, V_{ID} (see Note 2)		±30	±30	±30	V
Input voltage, V_I (see Notes 1 and 3)		±15	±15	±15	V
Duration of output short circuit (see Note 4)		unlimited	unlimited	unlimited	
Continuous total dissipation		See Dissipation Rating Table			
Operating free-air temperature range		0 to 70	–40 to 85	–55 to 125	°C
Storage temperature range		–65 to 150	–65 to 150	–65 to 150	°C
Case temperature for 60 seconds	FK package			260	°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds	J, JG, U, or W package			300	°C
Lead temperature 1,6 mm (1/6 inch) from case for 10 seconds	D, N, P, or PW package	260	260		°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values except differential voltages are with respect to the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at IN+ with respect to IN–.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 V, whichever is less.
4. The output may be shorted to ground or to either supply. Temperature and/or supply voltages must be limited to ensure that the dissipation rating is not exceeded.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR	DERATE ABOVE T_A	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D (8 pin)	680 mW	5.8 mW/°C	33°C	465 mW	378 mW	N/A
D (14 pin)	680 mW	7.6 mW/°C	60°C	604 mW	490 mW	N/A
FK	680 mW	11.0 mW/°C	88°C	680 mW	680 mW	273 mW
J	680 mW	11.0 mW/°C	88°C	680 mW	680 mW	273 mW
JG	680 mW	8.4 mW/°C	69°C	672 mW	546 mW	210 mW
N	680 mW	9.2 mW/°C	76°C	680 mW	597 mW	N/A
P	680 mW	8.0 mW/°C	65°C	640 mW	520 mW	N/A
PW (8 pin)	525 mW	4.2 mW/°C	25°C	336 mW	N/A	N/A
PW (14 pin)	700 mW	5.6 mW/°C	25°C	448 mW	N/A	N/A
U	675 mW	5.4 mW/°C	25°C	432 mW	351 m/W	135 mW
W	680 mW	8.0 mW/°C	65°C	640 mW	520 mW	200 mW

electrical characteristics, $V_{CC\pm}$ = ±15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		TL061C TL062C TL064C			TL061AC TL062AC TL064AC			TL061BC TL062BC TL064BC			TL061I TL062I TL064I			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 0, R_S = 50 Ω	T_A = 25°C		3	15		3	6		2	3		3	6	mV
			T_A = Full range			20			7.5			5			9	
α_{VIO}	Temperature coefficient of input offset voltage	V_O = 0, T_A = Full range	R_S = 50 Ω,		10			10			10			10		μV/°C
I_{IO}	Input offset current	V_O = 0	T_A = 25°C		5	200		5	100		5	100		5	100	pA
			T_A = Full range			5			3			3			10	nA
I_{IB}	Input bias current‡	V_O = 0	T_A = 25°C		30	400		30	200		30	200		30	200	pA
			T_A = Full range			10			7			7			20	nA
V_{ICR}	Common-mode input voltage range	T_A = 25°C		±11	−12 to 15		±11	−12 to 15		±11	−12 to 15		±11	−12 to 15		V
V_{OM}	Maximum peak output voltage swing	R_L = 10 kΩ,	T_A = 25°C	±10	±13.5		±10	±13.5		±10	±13.5		±10	±13.5		V
		R_L ≥ 10 kΩ,	T_A = Full range	±10			±10			±10			±10			
A_{VD}	Large-signal differential voltage amplification	V_O = ± 10 V, R_L ≥ 10 kΩ	T_A = 25°C	3	6		4	6		4	6		4	6		V/mV
			T_A = Full range	3			4			4			4			
B_1	Unity-gain bandwidth	R_L = 10 kΩ,	T_A = 25°C		1			1			1			1		MHz
r_i	Input resistance	T_A = 25°C			10^{12}			10^{12}			10^{12}			10^{12}		Ω
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$min, R_S = 50 Ω,	V_O = 0, T_A = 25°C	70	86		80	86		80	86		80	86		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	V_{CC} = ± 9 V to ± 15 V, V_O = 0, T_A = 25°C	R_S = 50 Ω,	70	95		80	95		80	95		80	95		dB
P_D	Total power dissipation (each amplifier)	V_O = 0, No load	T_A = 25°C,		6	7.5		6	7.5		6	7.5		6	7.5	mW
I_{CC}	Supply current (each amplifier)	V_O = 0, No load	T_A = 25°C,		200	250		200	250		200	250		200	250	μA
V_{O1}/V_{O2}	Crosstalk attenuation	A_{VD} = 100,	T_A = 25°C		120			120			120			120		dB

† All characteristics are measured under open-loop conditions with zero common-mode input voltage unless otherwise specified. Full range for T_A is 0°C to 70°C for TL06_C, TL06_AC, and TL06_BC and −40°C to 85°C for TL06_I.
‡ Input bias currents of a FET-input operational amplifier are normal junction reverse currents, which are temperature sensitive as shown in Figure 15. Pulse techniques must be used that will maintain the junction temperature as close to the ambient temperature as possible.

electrical characteristics, $V_{CC\pm}$ = ±15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		TL061M TL062M			TL064M			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 0, R_S = 50 Ω	T_A = 25°C		3	6		3	9	mV
			T_A = –55°C to 125°C			9			15	
α_{VIO}	Temperature coefficient of input offset voltage	V_O = 0, R_S = 50 Ω, T_A = –55°C to 125°C			10			10		μV/°C
I_{IO}	Input offset current	V_O = 0	T_A = 25°C		5	100		5	100	pA
			T_A = – 55°C to 125°C			20			20	nA
I_{IB}	Input bias current‡	V_O = 0	T_A = 25°C		30	200		30	200	pA
			T_A = – 55°C to 125°C			50			50	nA
V_{ICR}	Common-mode input voltage range	T_A = 25°C		±11.5	–12 to 15		±11.5	–12 to 15		V
V_{OM}	Maximum peak output voltage swing	R_L = 10 kΩ,	T_A = 25°C	±10	±13.5		±10	±13.5		V
		R_L ≥ 10 kΩ,	T_A = –55°C to 125°C	±10			±10			
A_{VD}	Large-signal differential voltage amplification	V_O = ±10 V, R_L ≥ 10 kΩ	T_A = 25°C	4	6		4	6		V/mV
			T_A = –55°C to 125°C	4			4			
B_1	Unity-gain bandwidth	R_L = 10 kΩ,	T_A = 25°C							MHz
r_i	Input resistance	T_A = 25°C			10^{12}			10^{12}		Ω
CMRR	Common-mode rejection ratio	V_{IC}= V_{ICR}min, V_O = 0, R_S = 50 Ω, T_A = 25°C		80	86		80	86		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	V_{CC}= ±9 V to ±15 V, V_O = 0, R_S = 50 Ω, T_A = 25°C		80	95		80	95		dB
P_D	Total power dissipation (each amplifier)	V_O = 0, T_A = 25°C, No load			6	7.5		6	7.5	mW
I_{CC}	Supply current (each amplifier)	V_O = 0, T_A = 25°C, No load			200	250		200	250	μA
V_{O1}/V_{O2}	Crosstalk attenuation	A_{VD} = 100,	T_A = 25°C		120			120		dB

† All characteristics are measured under open-loop conditions with zero common-mode voltage unless otherwise specified.
‡ Input bias currents of a FET-input operational amplifier are normal junction reverse currents, which are temperature sensitive as shown in Figure 15. Pulse techniques must be used that maintain the junction temperature as close to the ambient temperature as possible.

operating characteristics, $V_{CC\pm}$ = ±15 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain (see Note 5)	V_I = 10 V, C_L = 100 pF,	R_L = 10 kΩ, See Figure 1	1.5	3.5		V/μs
t_r	Rise time	V_I = 20 V, C_L = 100 pF,	R_L = 10 kΩ, See Figure 1		0.2		μs
	Overshoot factor				10%		
V_n	Equivalent input noise voltage	R_S = 20 Ω,	f = 1 kHz		42		nV/√Hz

NOTE 5: Slew rate at –55°C to 125°C is 0.7 V/μs min.

electrical characteristics, $V_{CC\pm} = \pm 15$ V, $T_A = 25°C$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		TL061Y TL062Y TL064Y MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	$V_O = 0$,	$R_S = 50\ \Omega$		3	15	mV
α_{VIO}	Temperature coefficient of input offset voltage	$V_O = 0$,	$R_S = 50\ \Omega$		10		μV/°C
I_{IO}	Input offset current	$V_O = 0$			5	200	pA
I_{IB}	Input bias current‡	$V_O = 0$			30	400	pA
V_{ICR}	Common-mode input voltage range			±11	–12 to 15		V
V_{OM}	Maximum peak output voltage swing	$R_L = 10\ k\Omega$		±10	±13.5		V
A_{VD}	Large-signal differential voltage amplification	$V_O = \pm 10$ V,	$R_L \geq 2\ k\Omega$	3	6		V/mV
B_1	Unity-gain bandwidth	$R_L = 10\ k\Omega$			1		MHz
r_i	Input resistance				10^{12}		Ω
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$min, $R_S = 50\ \Omega$	$V_O = 0$,	70	86		dB
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{CC\pm} / \Delta V_{IO}$)	$V_{CC} = \pm 9$ V to ± 15 V, $R_S = 50\ \Omega$	$V_O = 0$,	70	95		dB
P_D	Total power dissipation (each amplifier)	$V_O = 0$,	No load		6	7.5	mW
I_{CC}	Supply current (per amplifier)	$V_O = 0$,	No load		200	250	μA
V_{O1}/V_{O2}	Crosstalk attenuation	$A_{VD} = 100$			120		dB

† All characteristics are measured under open-loop conditions with zero common-mode voltage unless otherwise specified.
‡ Input bias currents of a FET-input operational amplifier are normal junction reverse currents, which are temperature sensitive as shown in Figure 15. Pulse techniques must be used that maintain the junction temperature as close to the ambient temperature as possible.

operating characteristics, $V_{CC\pm} = \pm 15$ V, $T_A = 25°C$

PARAMETER		TEST CONDITIONS		TL061Y TL062Y TL064Y MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	$V_I = 10$ mV, $C_L = 100$ pF,	$R_L = 10\ k\Omega$, See Figure 1	1.5	3.5		V/μs
t_r	Rise time	$V_I = 20$ V, $C_L = 100$ pF,	$R_L = 10\ k\Omega$, See Figure 1		0.2		μs
	Overshoot factor				10%		
V_n	Equivalent input noise voltage	$R_S = 20\ \Omega$,	f = 1 kHz		42		nV/√Hz

PARAMETER MEASUREMENT INFORMATION

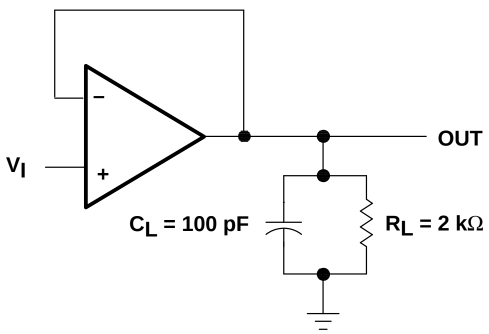


Figure 1. Unity-Gain Amplifier

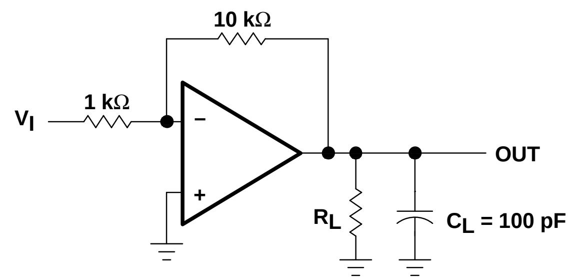


Figure 2. Gain-of-10 Inverting Amplifier

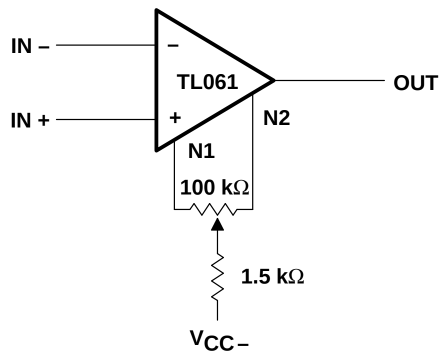


Figure 3. Input Offset Voltage Null Circuit

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
V_{OM}	Maximum output voltage	vs Supply voltage vs Free-air temperature vs Load resistance vs Frequency	4 5 6 7
A_{VD}	Differential voltage amplification	vs Free-air temperature	8
A_{VD}	Large-signal differential voltage amplification	vs Frequency	9
	Phase shift	vs Frequency	9
I_{CC}	Supply current	vs Supply voltage vs Free-air temperature	10 11
P_D	Total power dissipation	vs Free-air temperature	12
CMRR	Common-mode rejection ratio	vs Free-air temperature	13
	Normalized unity-gain bandwidth	vs Free-air temperature	14
	Normalized slew rate	vs Free-air temperature	14
	Normalized phase shift	vs Free-air temperature	14
I_{IB}	Input bias current	vs Free-air temperature	15
	Large-signal pulse response	vs Time	16
V_O	Output voltage	vs Elapsed time	17
V_n	Equivalent input noise voltage	vs Frequency	18

TYPICAL CHARACTERISTICS†

MAXIMUM PEAK OUTPUT VOLTAGE vs SUPPLY VOLTAGE

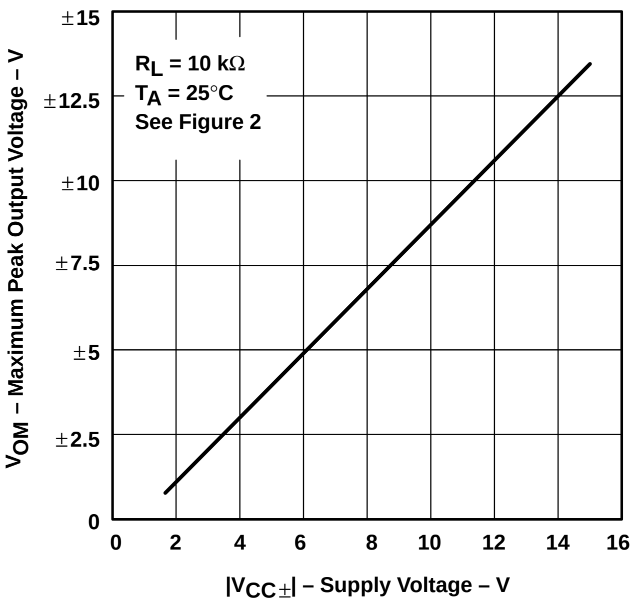


Figure 4

MAXIMUM PEAK OUTPUT VOLTAGE vs FREE-AIR TEMPERATURE

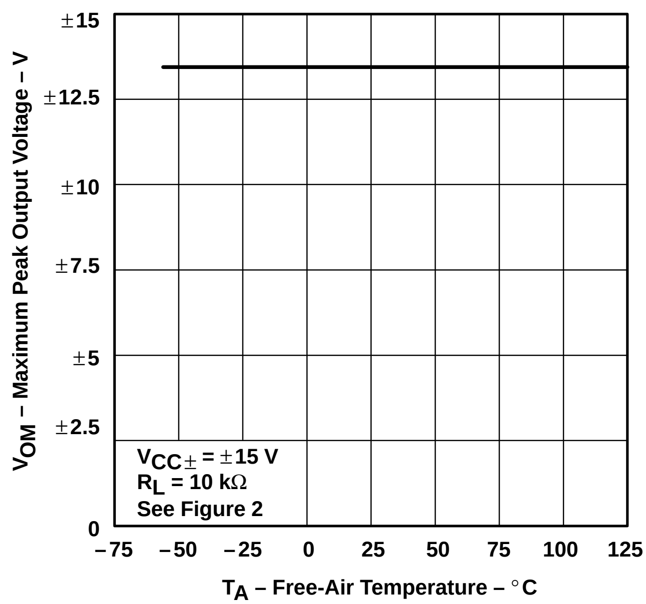


Figure 5

MAXIMUM PEAK OUTPUT VOLTAGE vs LOAD RESISTANCE

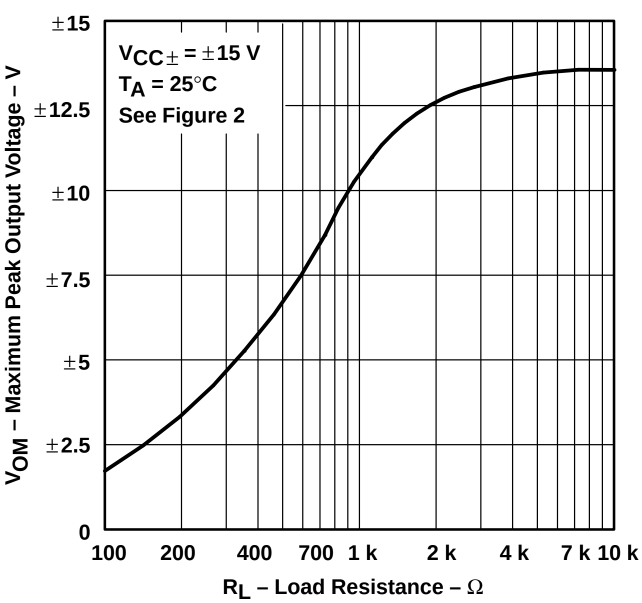


Figure 6

MAXIMUM PEAK OUTPUT VOLTAGE vs FREQUENCY

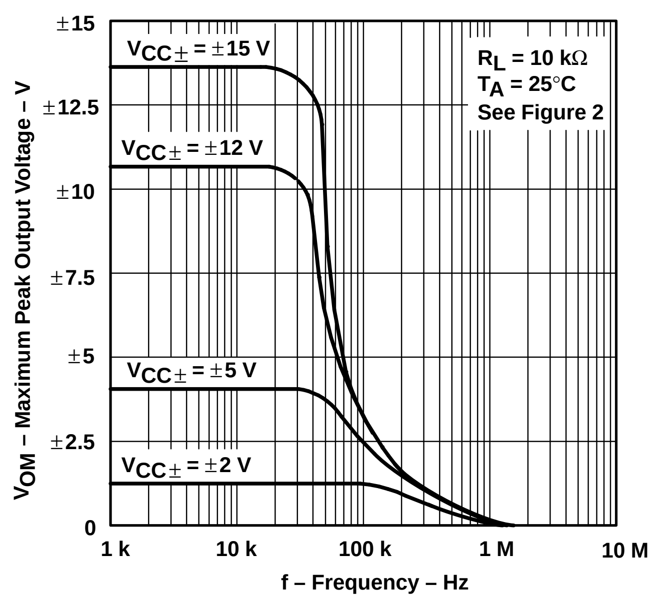


Figure 7

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

**DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
FREE-AIR TEMPERATURE**

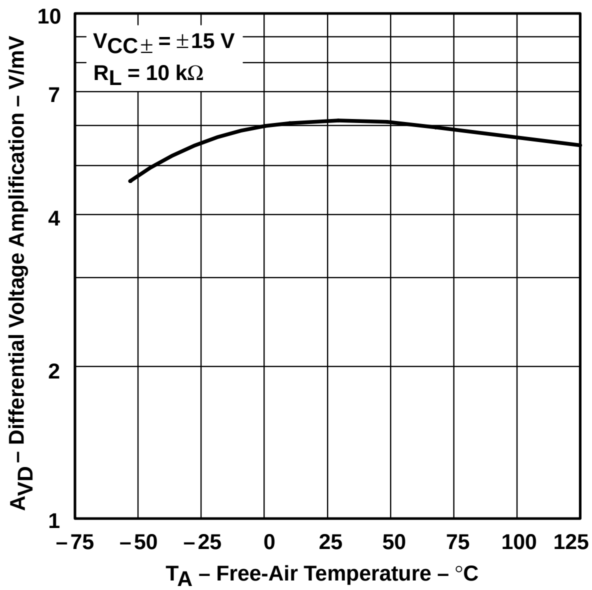


Figure 8

**LARGE-SIGNAL
DIFFERENTIAL VOLTAGE
AMPLIFICATION AND PHASE SHIFT
vs
FREQUENCY**

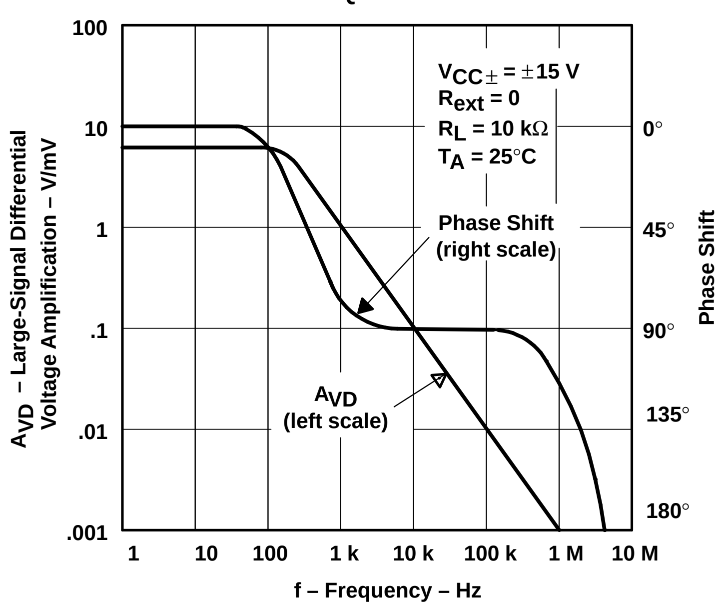


Figure 9

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

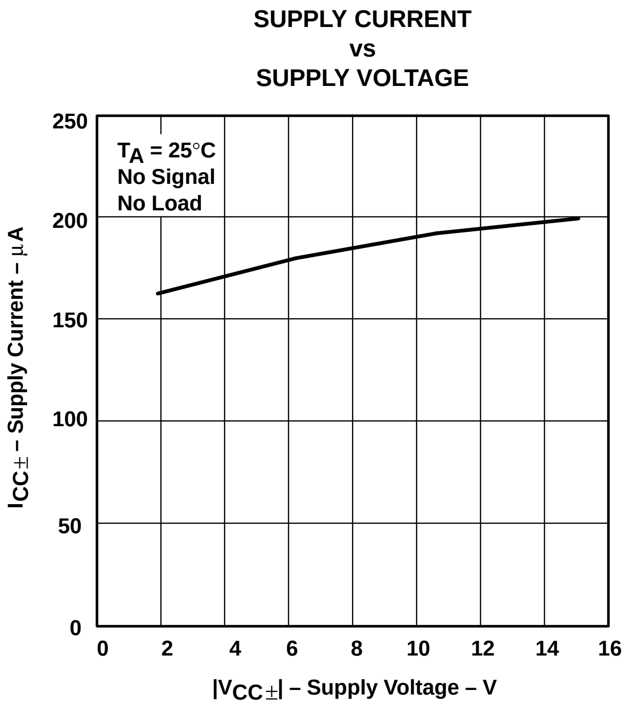


Figure 10

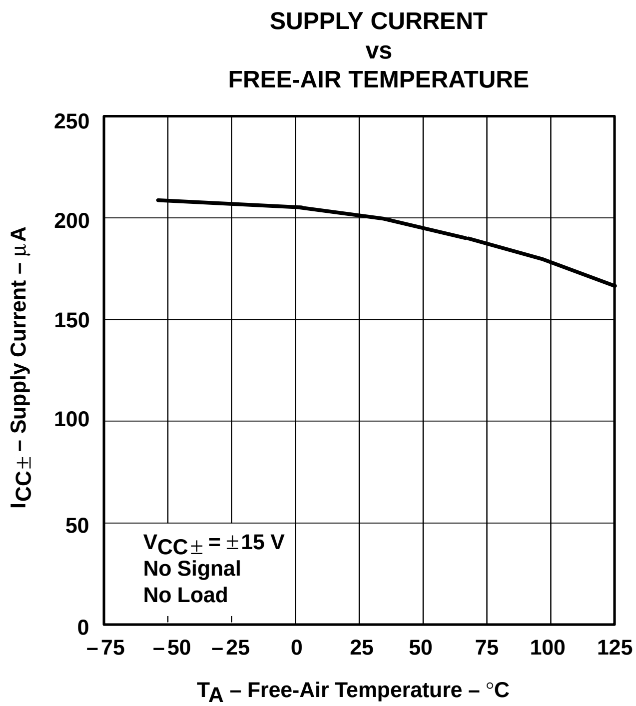


Figure 11

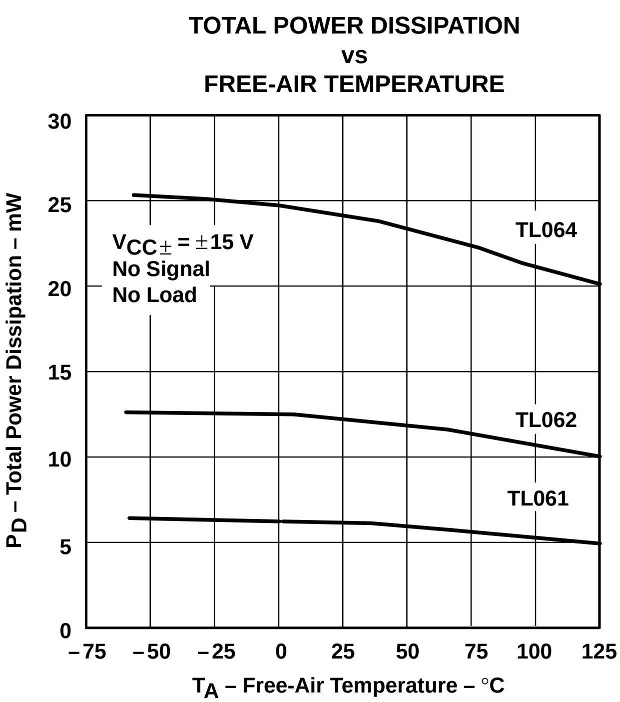


Figure 12

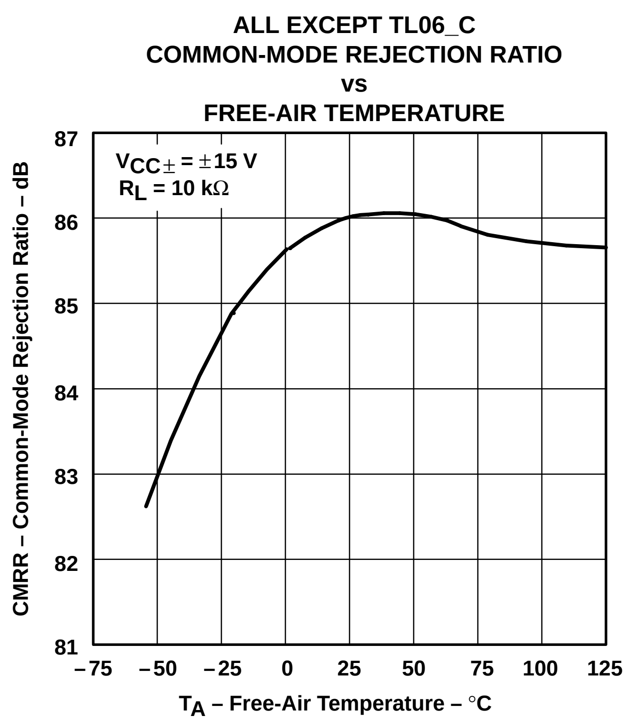


Figure 13

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

NORMALIZED UNITY GAIN BANDWIDTH SLEW RATE, AND PHASE SHIFT vs FREE-AIR TEMPERATURE

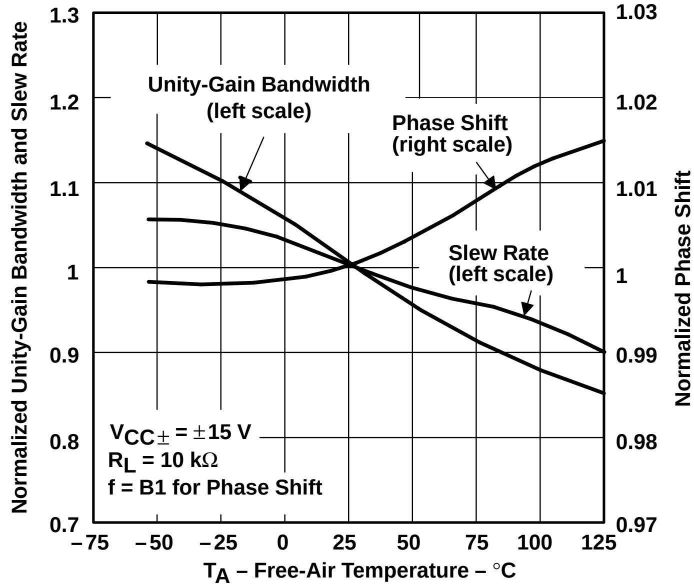


Figure 14

INPUT BIAS CURRENT vs FREE-AIR TEMPERATURE

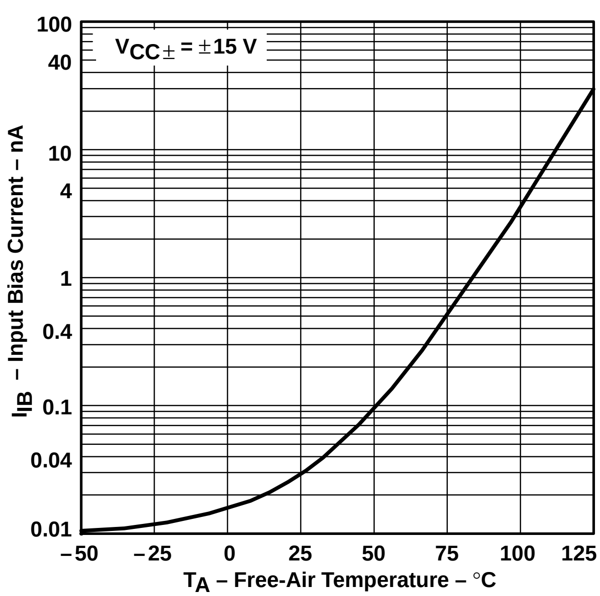


Figure 15

VOLTAGE FOLLOWER LARGE SIGNAL PULSE RESPONSE

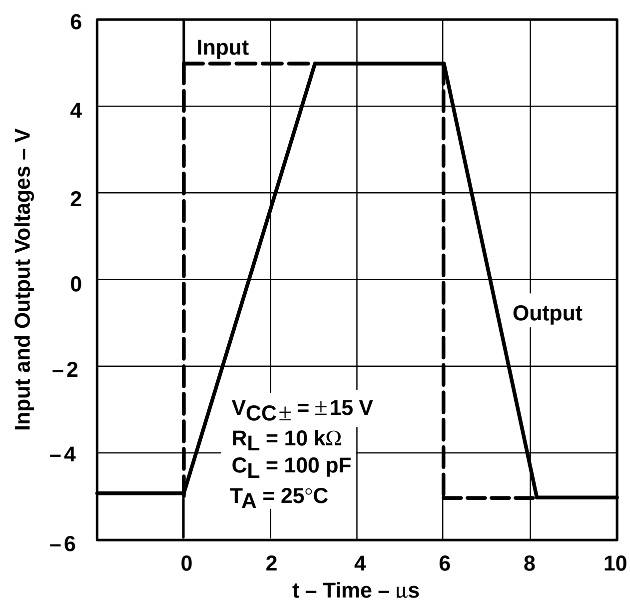


Figure 16

TYPICAL CHARACTERISTICS

OUTPUT VOLTAGE vs ELAPSED TIME

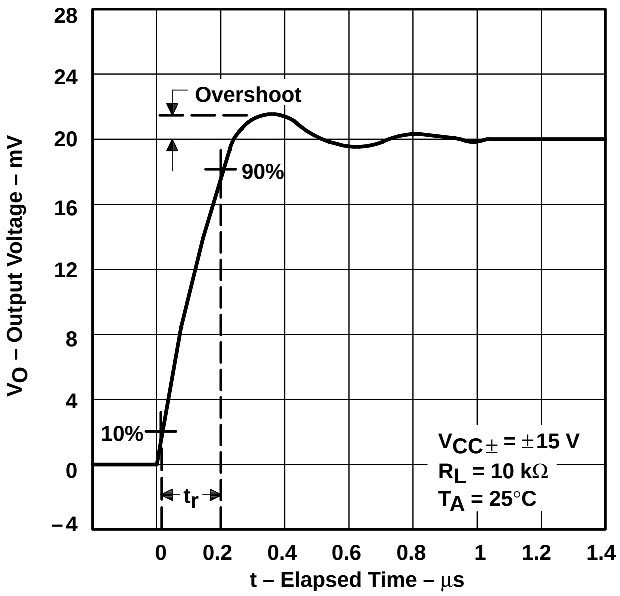


Figure 17

EQUIVALENT INPUT NOISE VOLTAGE vs FREQUENCY

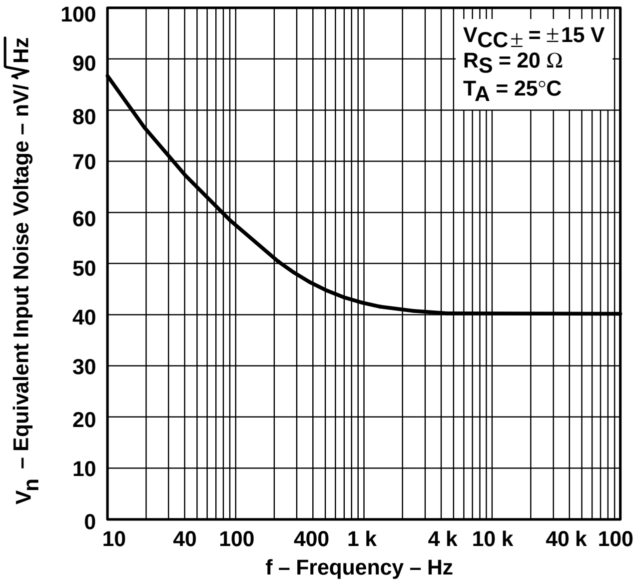


Figure 18

APPLICATION INFORMATION

Table of Application Diagrams

APPLICATION DIAGRAM	PART NUMBER	FIGURE
Instrumentation filter	TL064	19
0.5-Hz square-wave oscillator	TL061	20
High-Q notch filter	TL061	21
Audio-distribution amplifier	TL064	22
Low-level light detector preamplifier	TL061	23
AC amplifier	TL061	24
Microphone preamplifier with tone control	TL061	25
Instrumentation amplifier	TL062	26
IC preamplifier	TL062	27

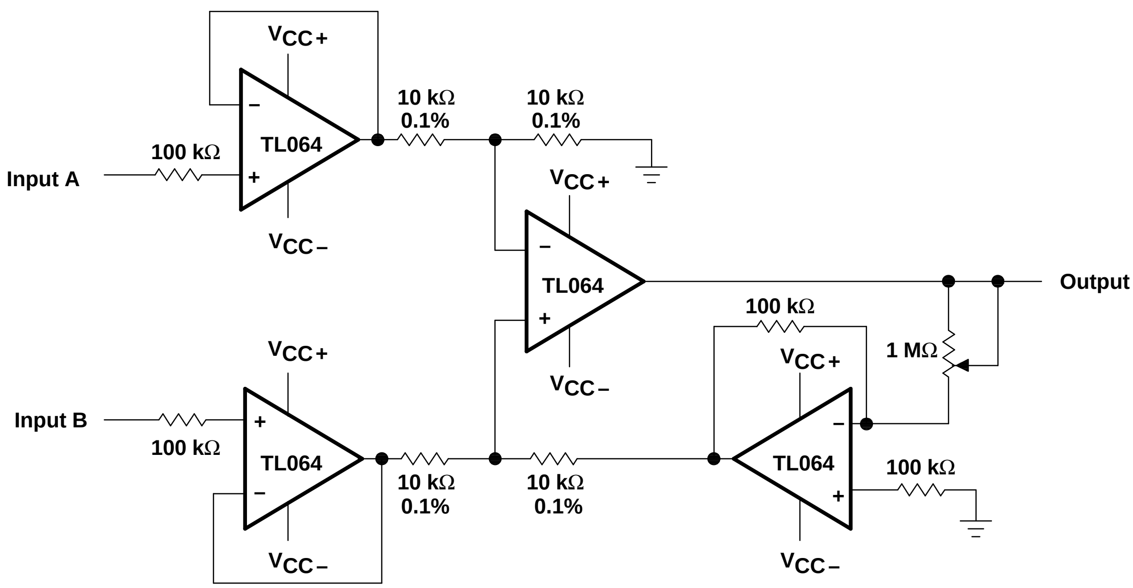


Figure 19. Instrumentation Amplifier

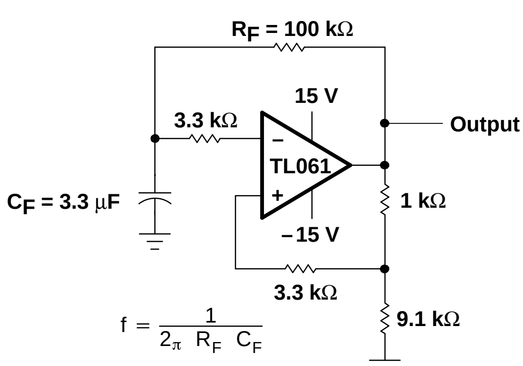


Figure 20. A 0.5-Hz Square-Wave Oscillator

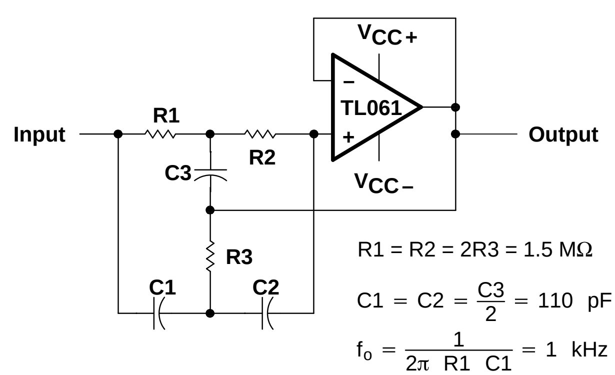


Figure 21. High-Q Nothc Filter

APPLICATION INFORMATION

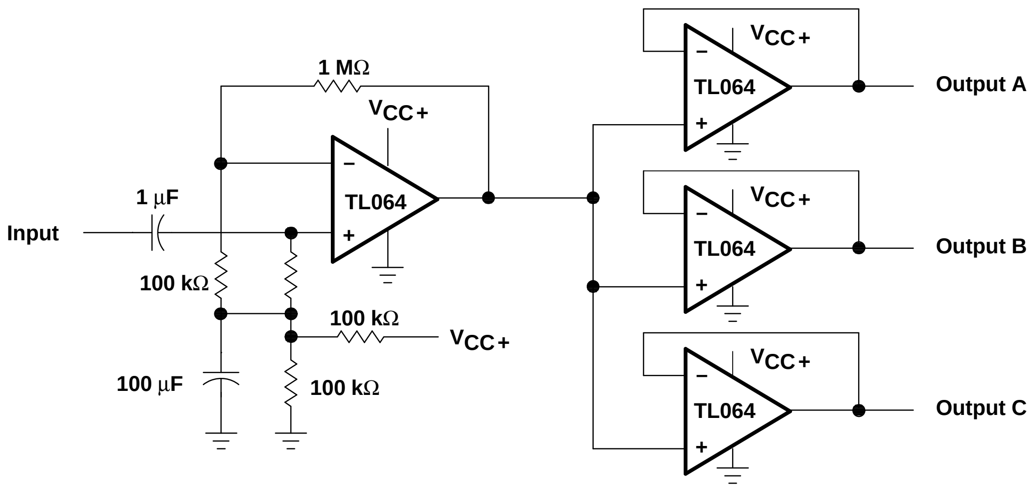


Figure 22. Audio-Distribution Amplifier

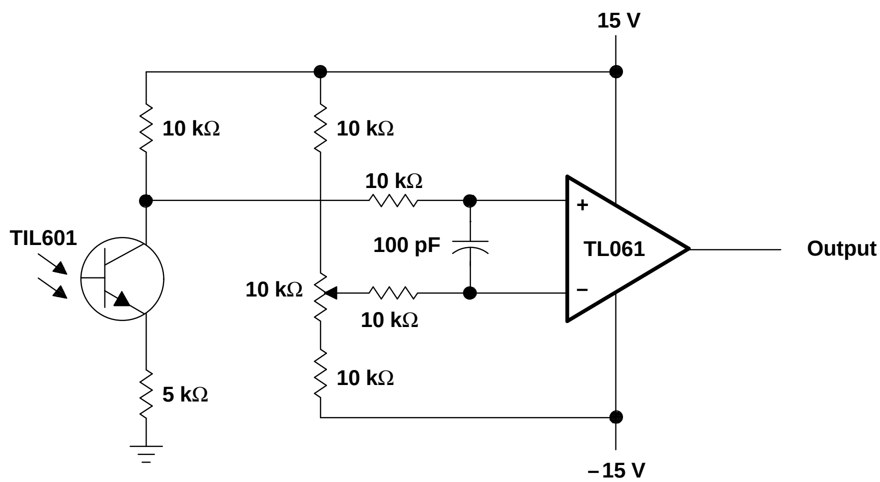


Figure 23. Low-Level Light-Detector Preamplifier

APPLICATION INFORMATION

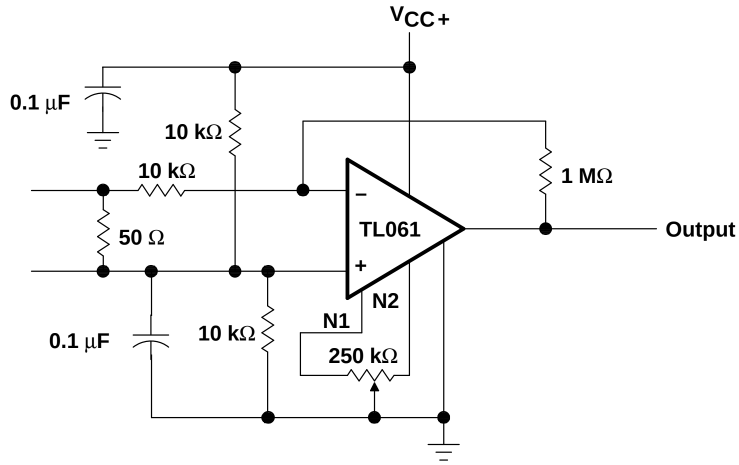


Figure 24. AC Amplifier

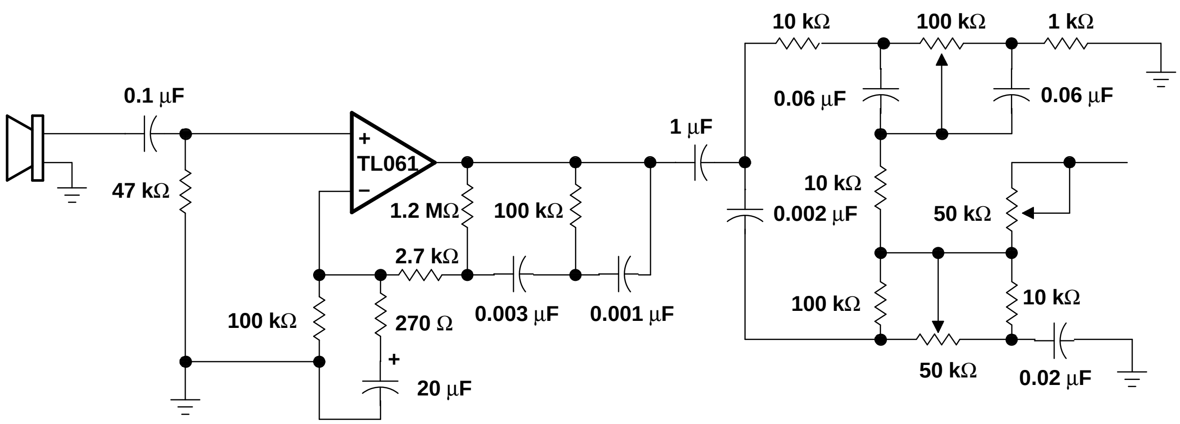


Figure 25. Microphone Preamplifier With Tone Control

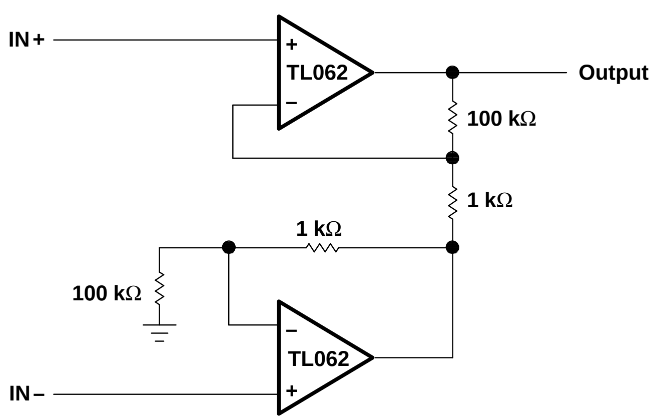
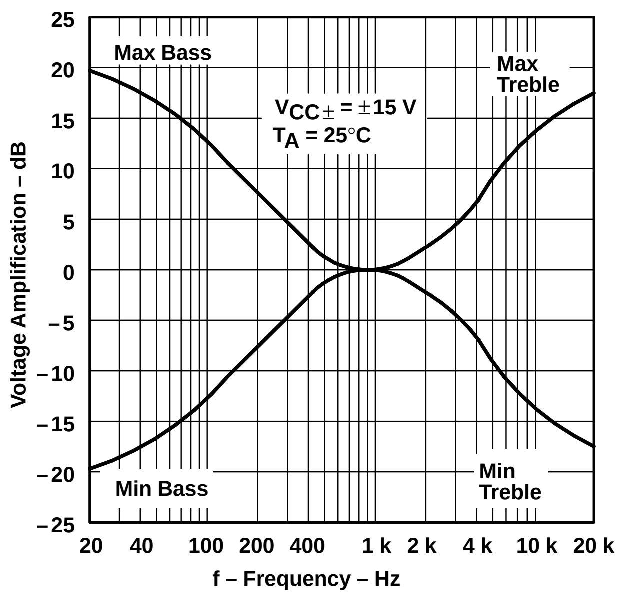


Figure 26. Instrumentation Amplifier

APPLICATION INFORMATION



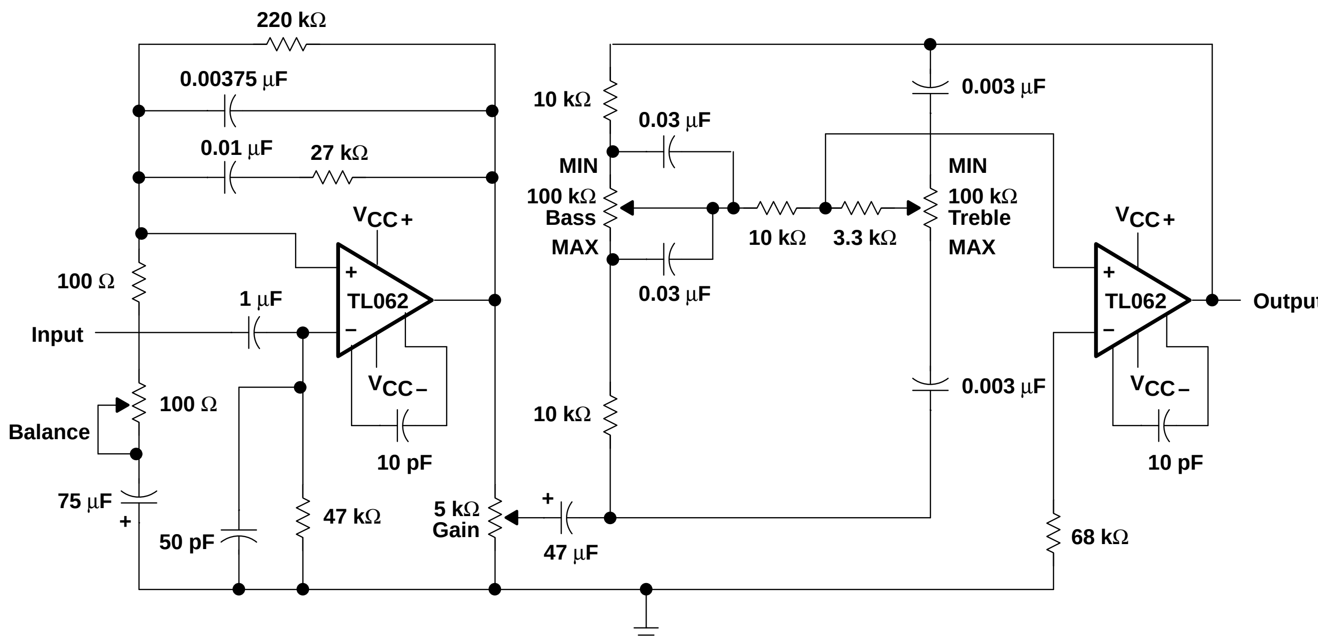


Figure 27. IC Preamplifier

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